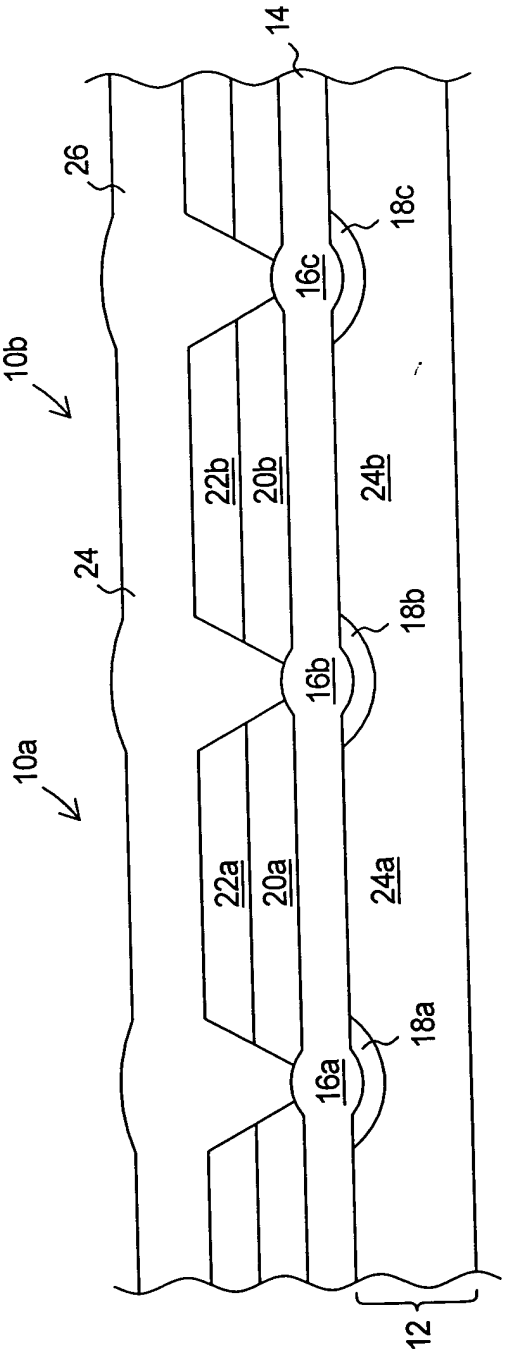


FIG. 1a
Prior Art

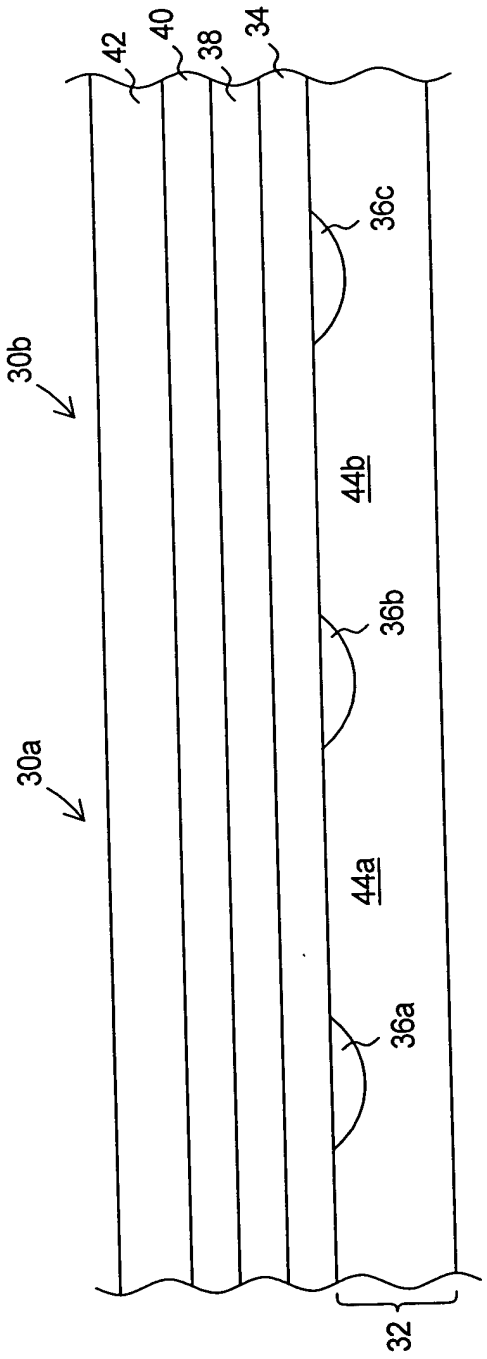


FIG. 1b
Prior Art

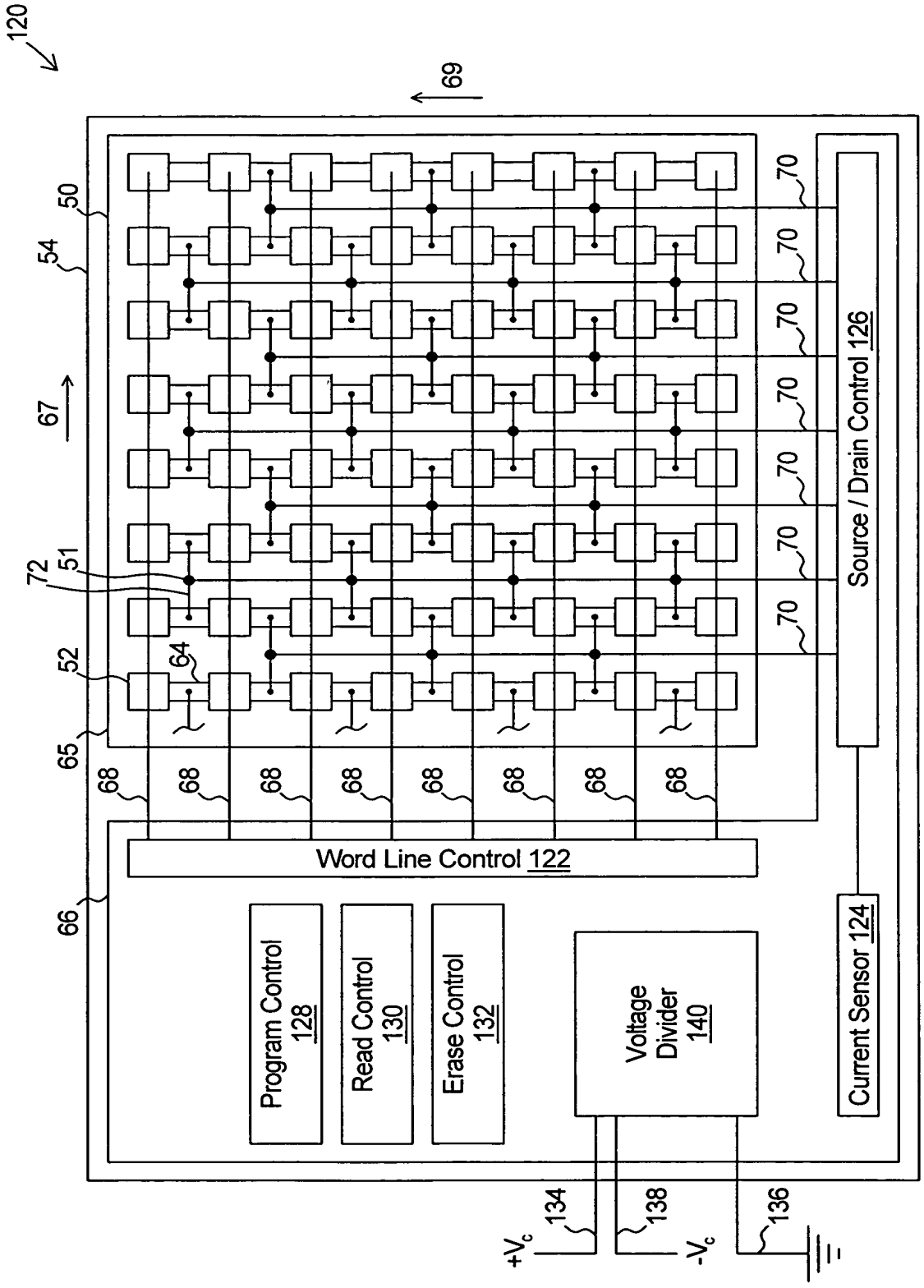

120
69
67
50
54
72
51
52
64
65
68
66
70
Source / Drain Control 126
Word Line Control 122
Program Control 128
Read Control 130
Erase Control 132
Voltage Divider 140
Current Sensor 124
134
138
136
+Vc
-Vc

Figure 2

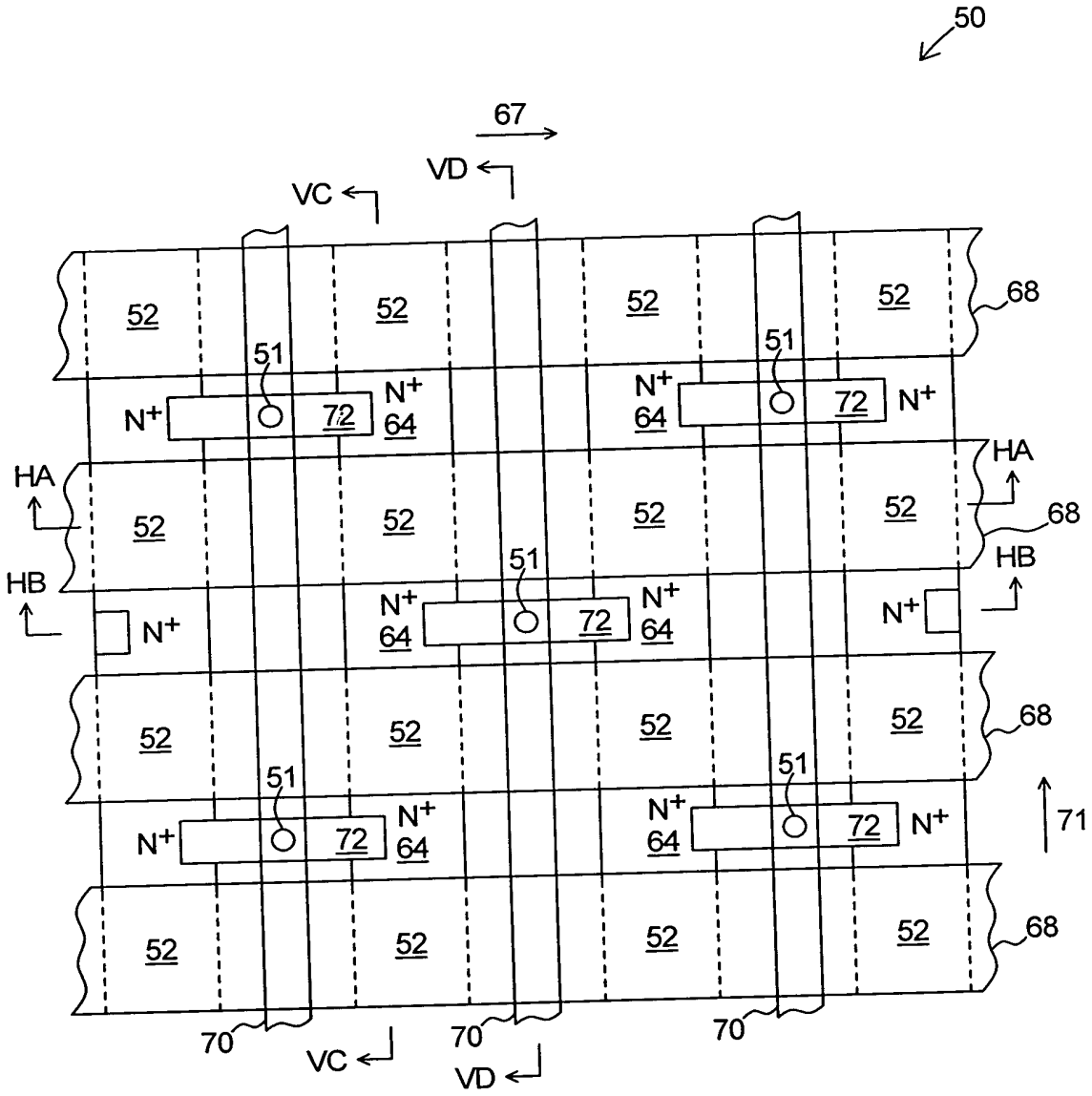


Figure 3

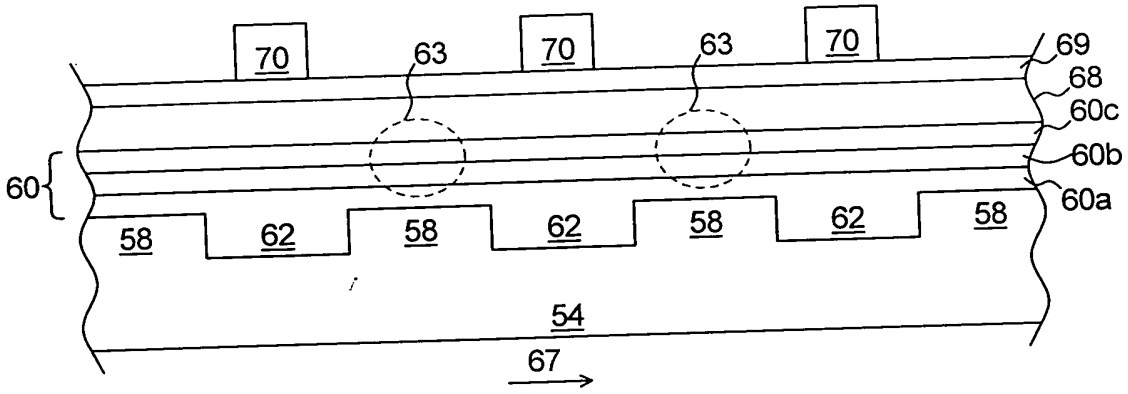


Figure 4a

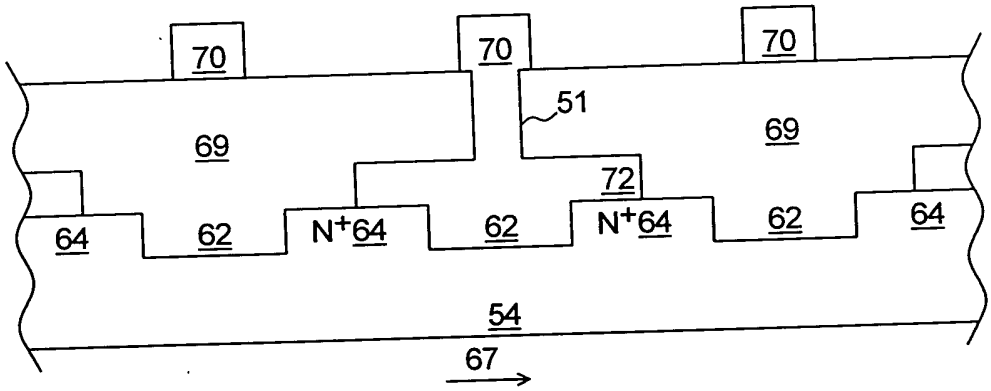


Figure 4b

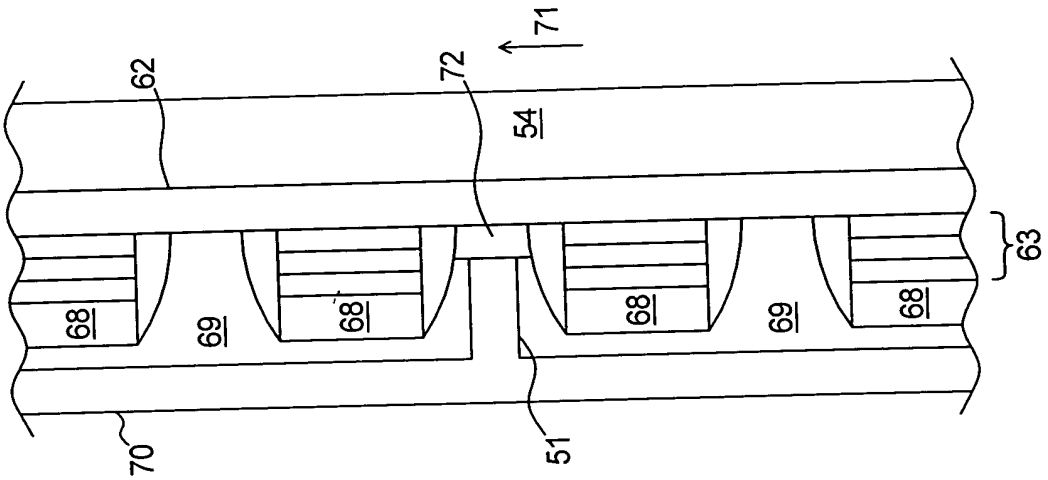


Figure 4d

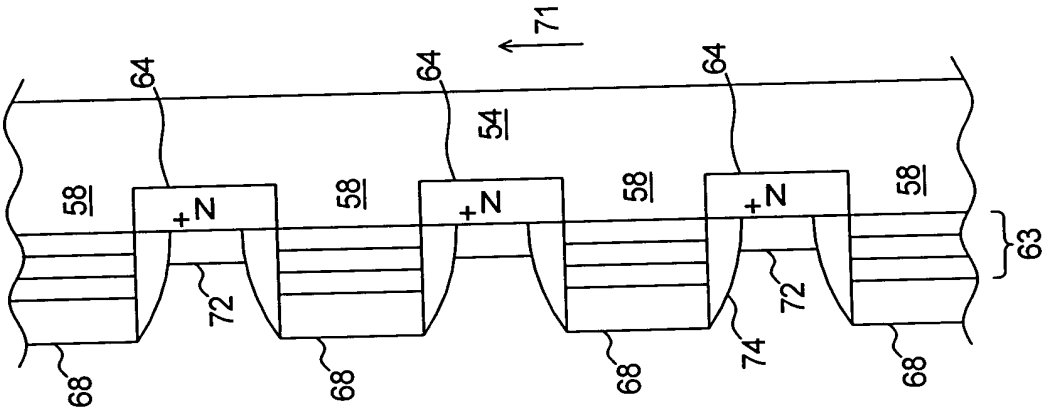


Figure 4c

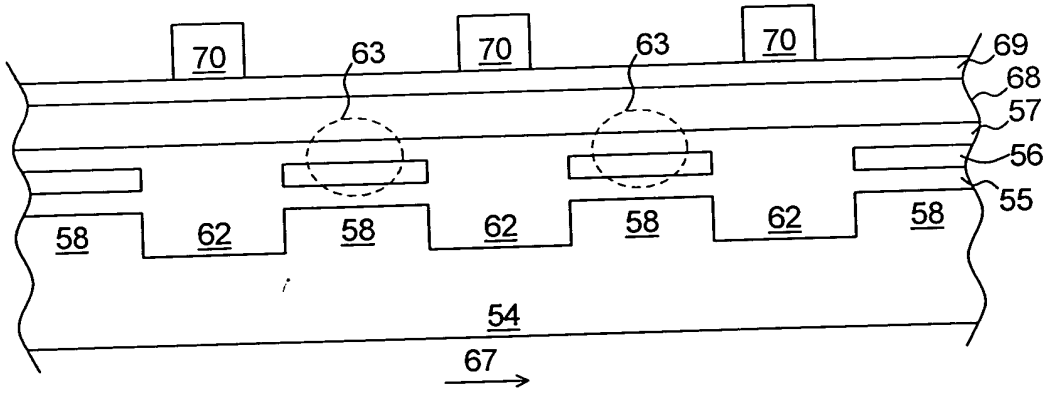


Figure 5a

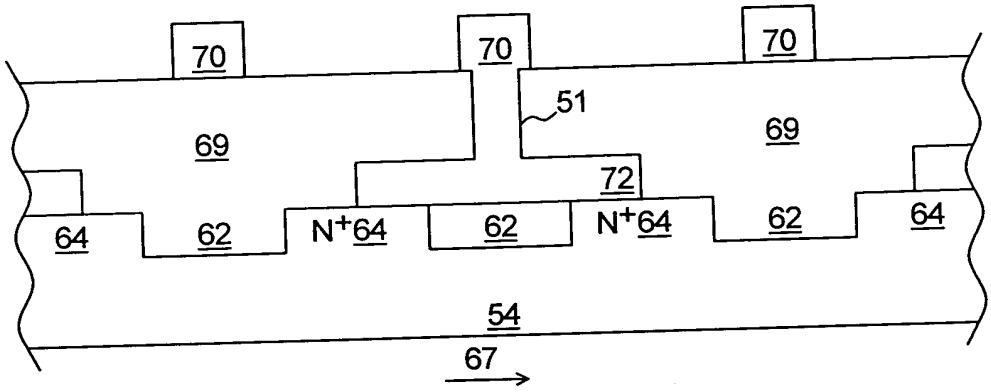


Figure 5b

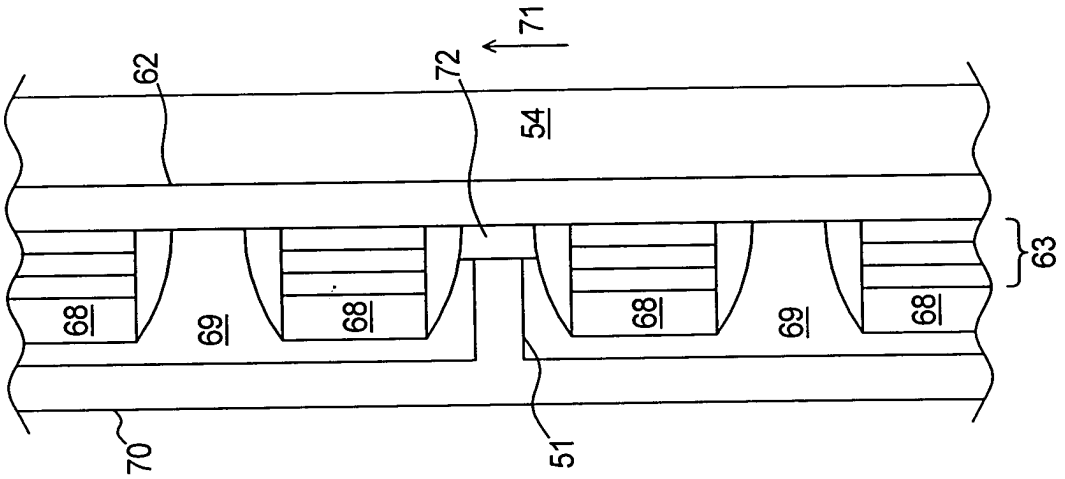


Figure 5d

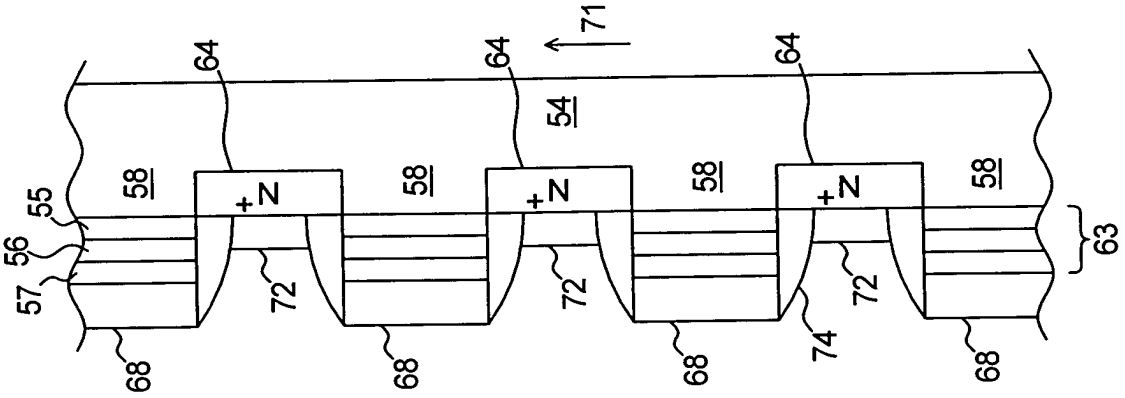


Figure 5c

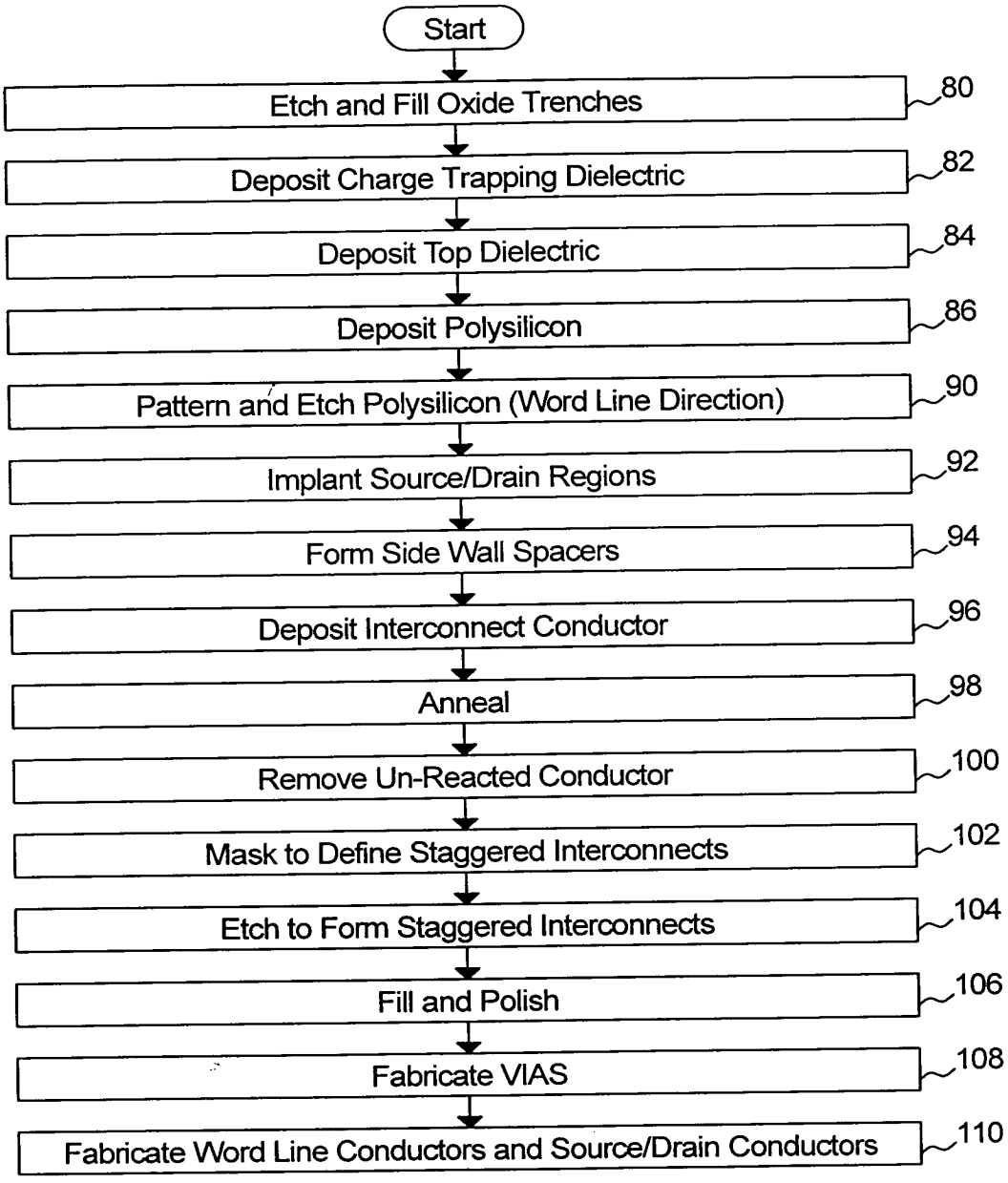

Start
Etch and Fill Oxide Trenches
80
Deposit Charge Trapping Dielectric
82
Deposit Top Dielectric
84
Deposit Polysilicon
86
Pattern and Etch Polysilicon (Word Line Direction)
90
Implant Source/Drain Regions
92
Form Side Wall Spacers
94
Deposit Interconnect Conductor
96
Anneal
98
Remove Un-Reacted Conductor
100
Mask to Define Staggered Interconnects
102
Etch to Form Staggered Interconnects
104
Fill and Polish
106
Fabricate VIAS
108
Fabricate Word Line Conductors and Source/Drain Conductors
110

Figure 6

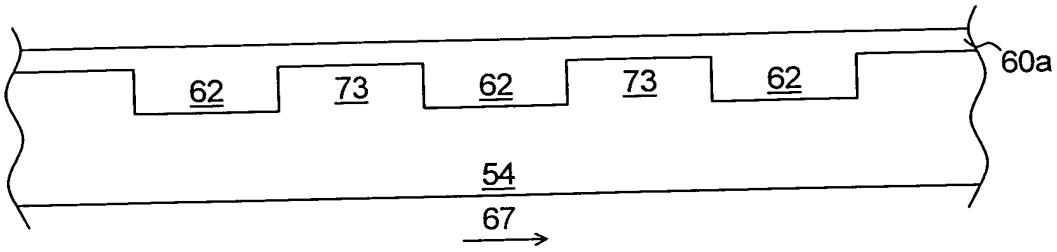


Figure 7

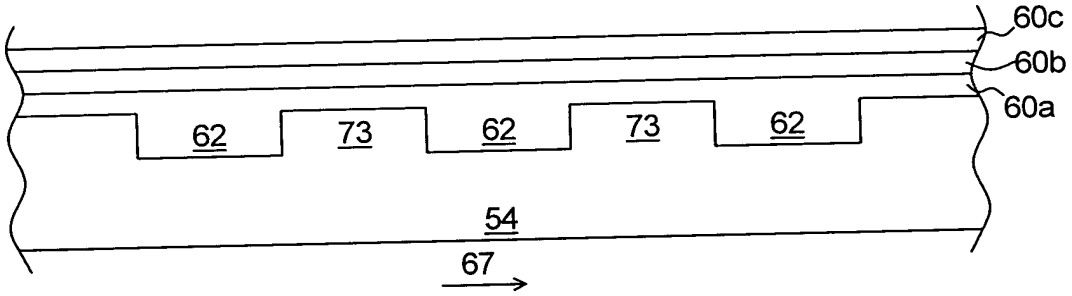


Figure 8

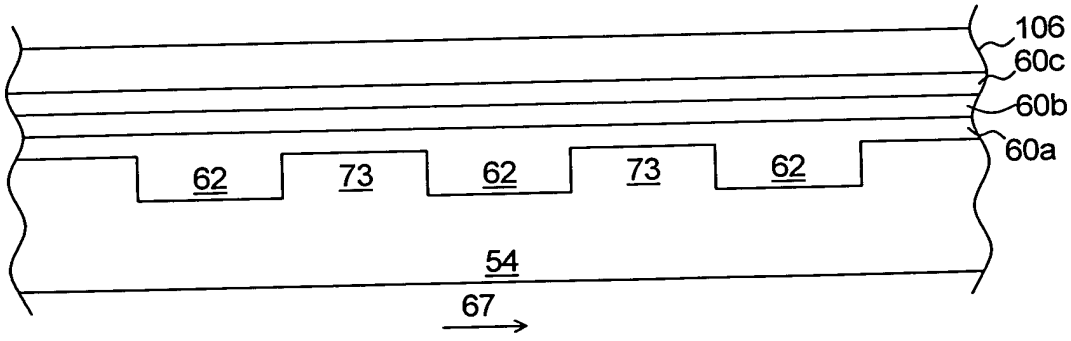


Figure 9

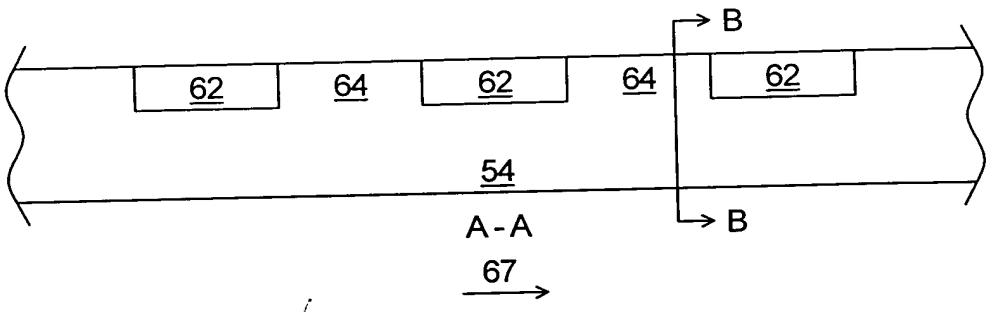


Figure 10a

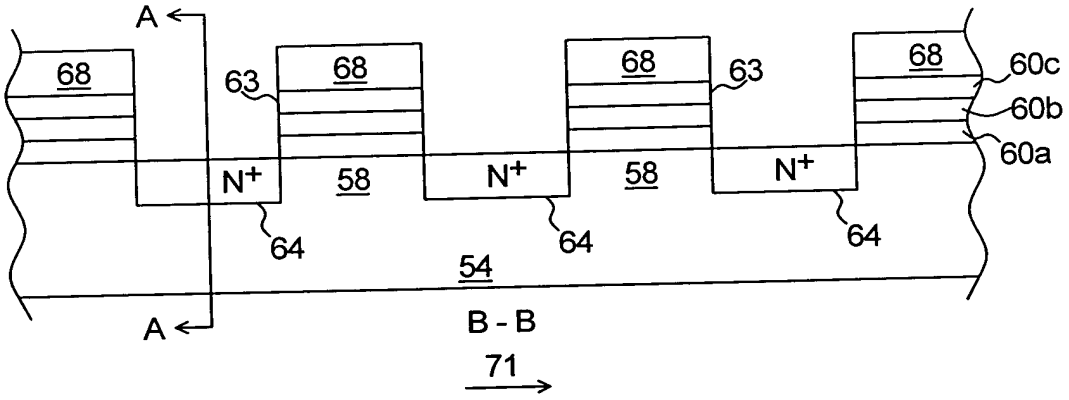


Figure 10b

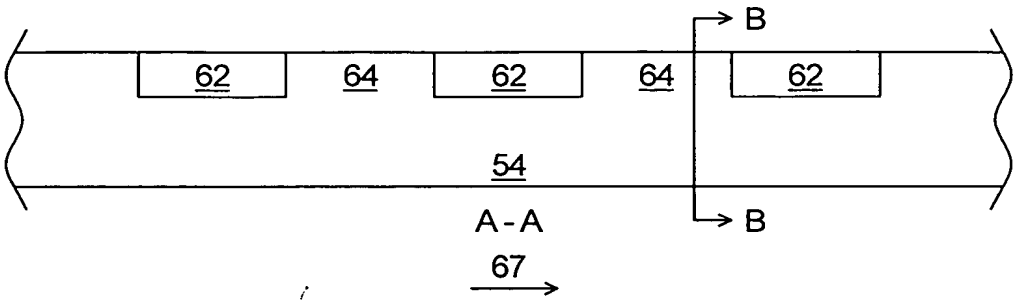


Figure 11a

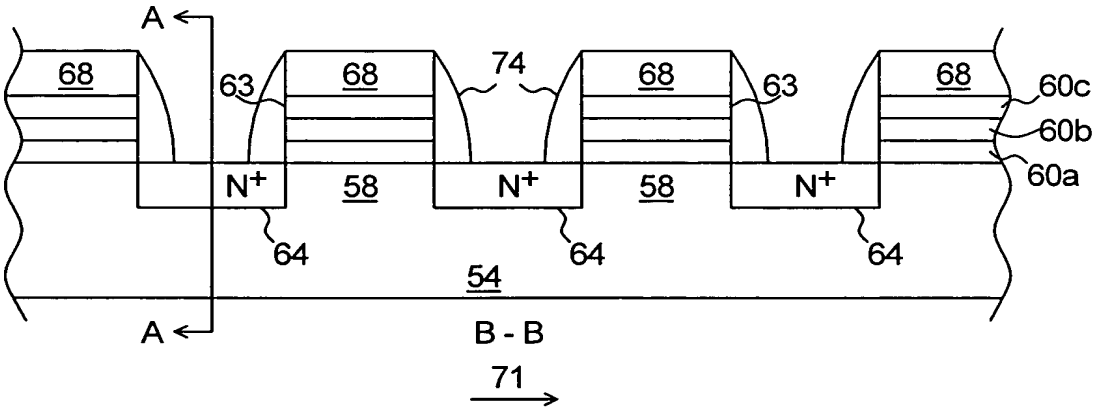


Figure 11b

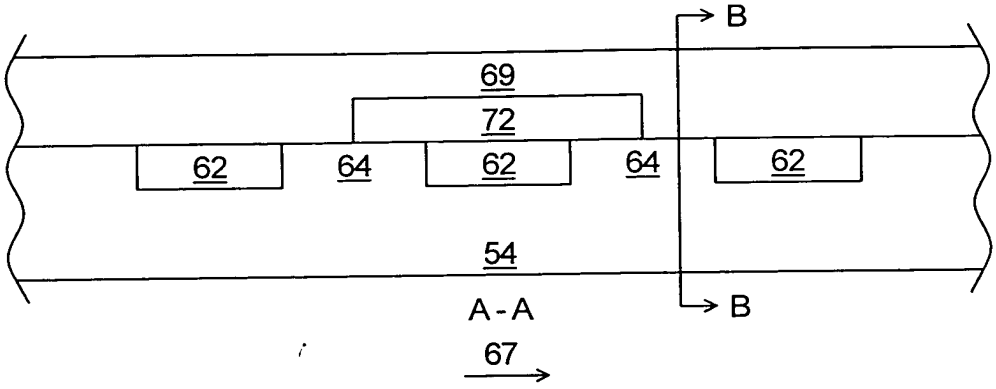


Figure 12a

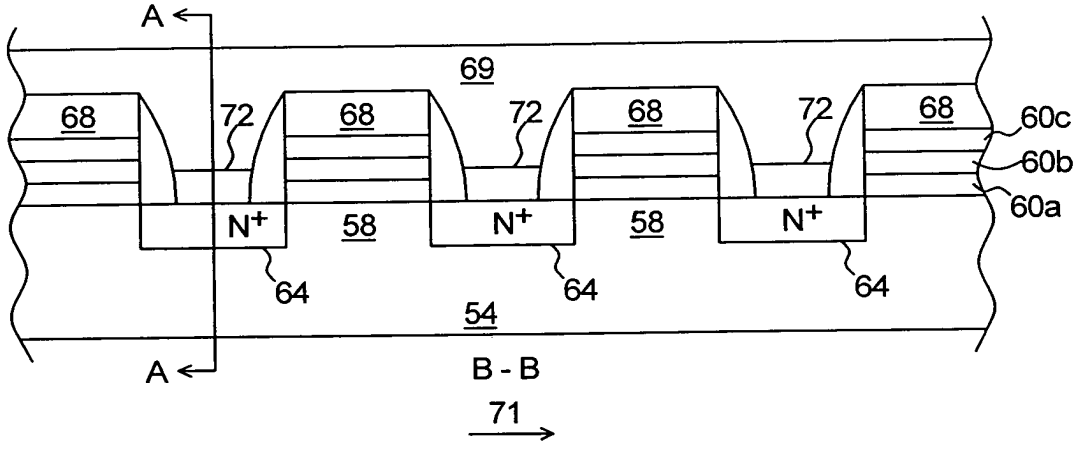


Figure 12b

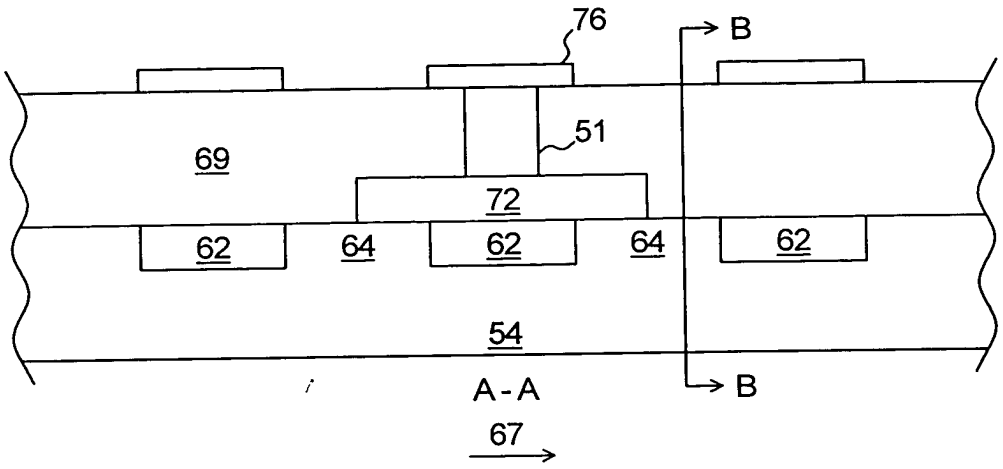


Figure 13a

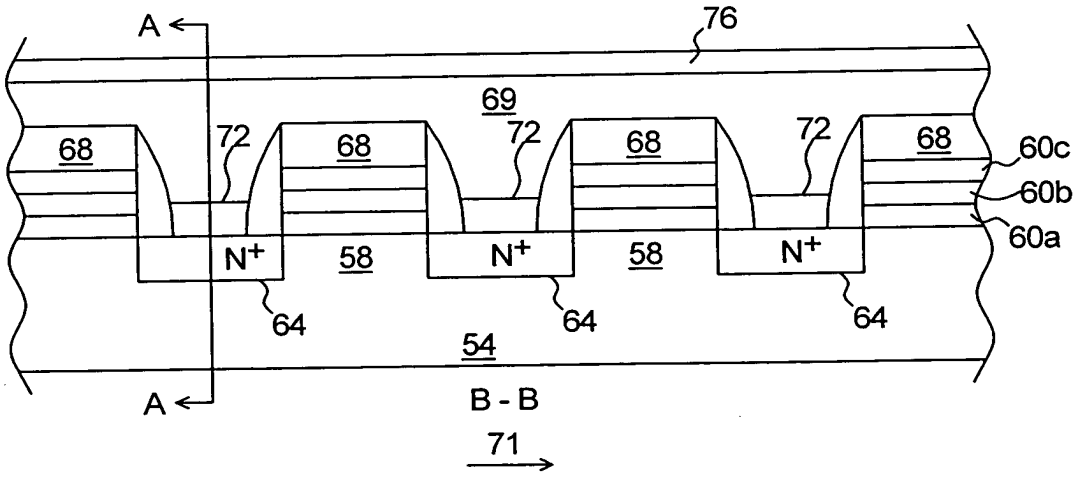


Figure 13b

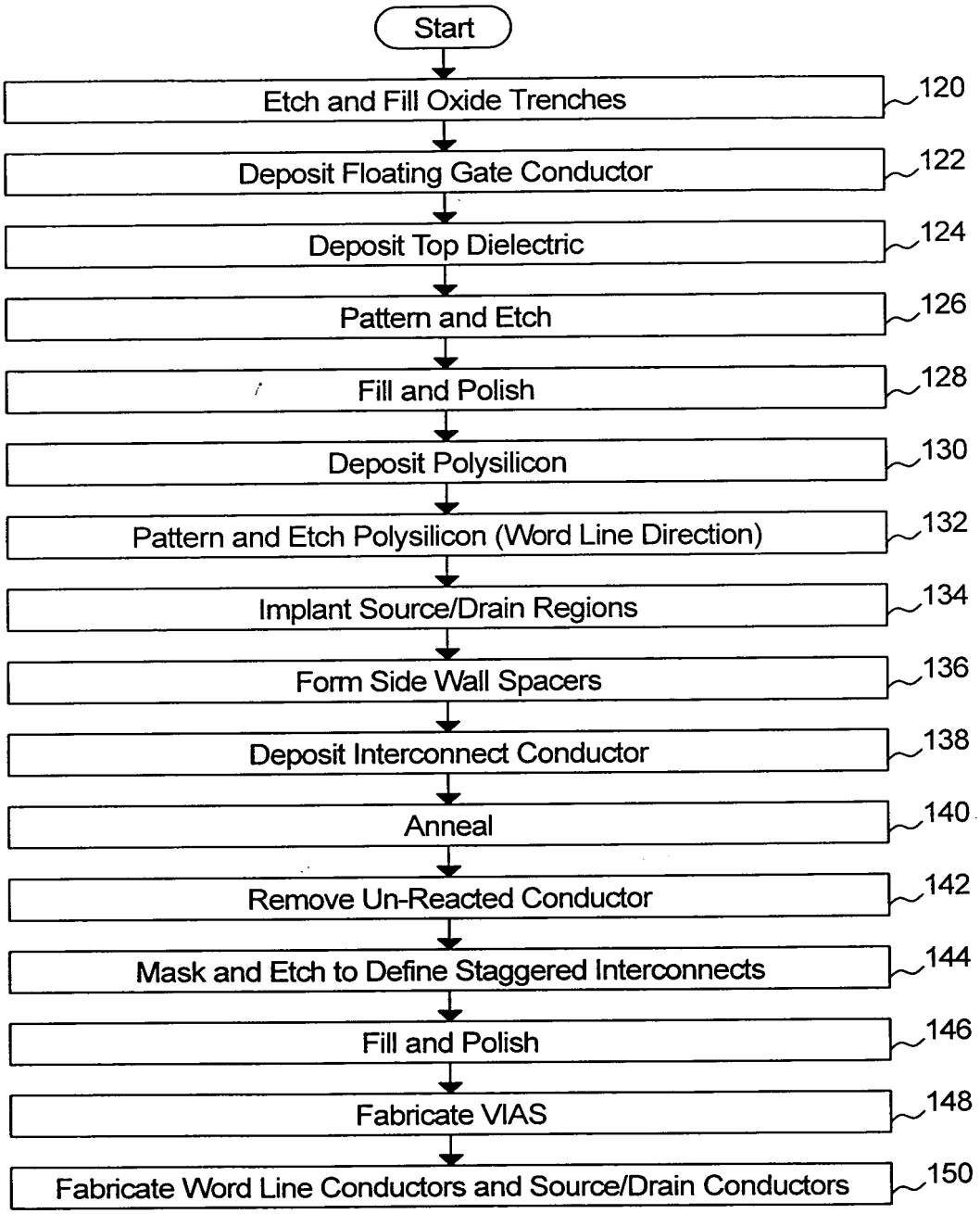

Start
Etch and Fill Oxide Trenches
120
Deposit Floating Gate Conductor
122
Deposit Top Dielectric
124
Pattern and Etch
126
Fill and Polish
128
Deposit Polysilicon
130
Pattern and Etch Polysilicon (Word Line Direction)
132
Implant Source/Drain Regions
134
Form Side Wall Spacers
136
Deposit Interconnect Conductor
138
Anneal
140
Remove Un-Reacted Conductor
142
Mask and Etch to Define Staggered Interconnects
144
Fill and Polish
146
Fabricate VIAS
148
Fabricate Word Line Conductors and Source/Drain Conductors
150

Figure 14

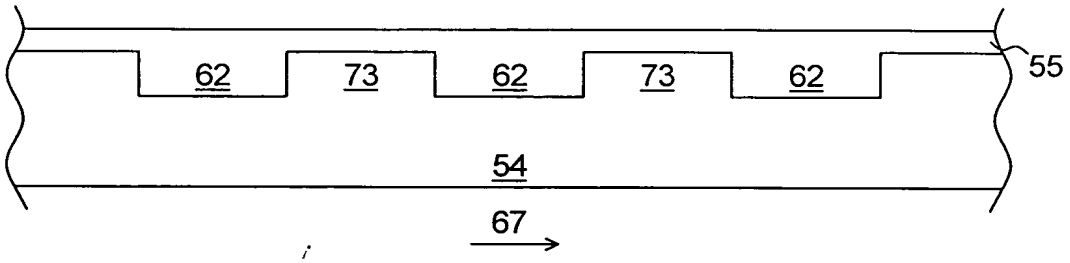


Figure 15

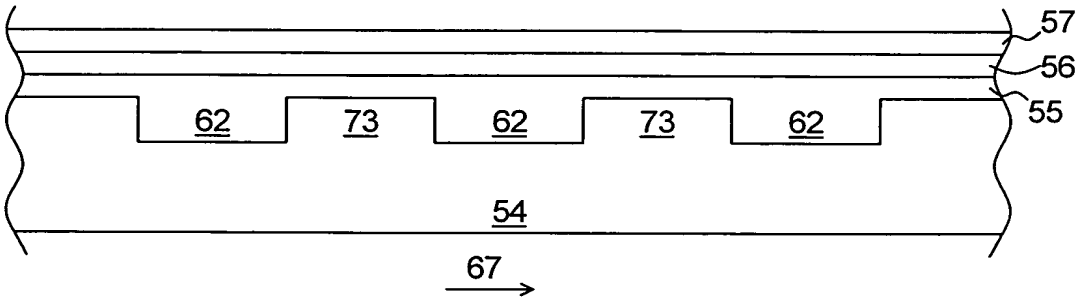


Figure 16

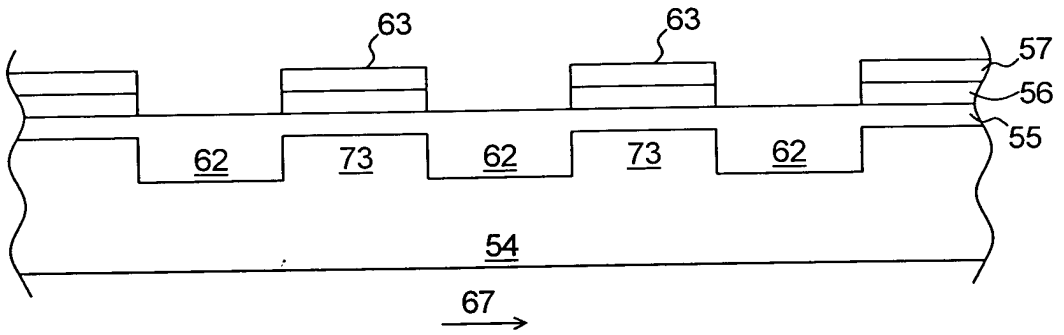


Figure 17

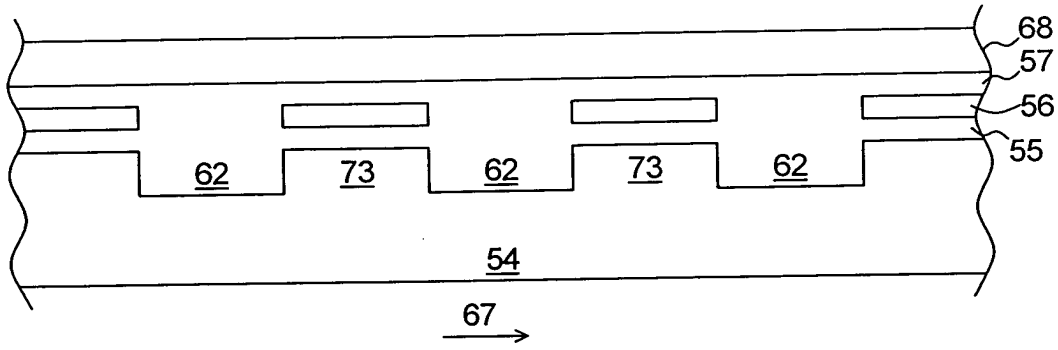


Figure 18

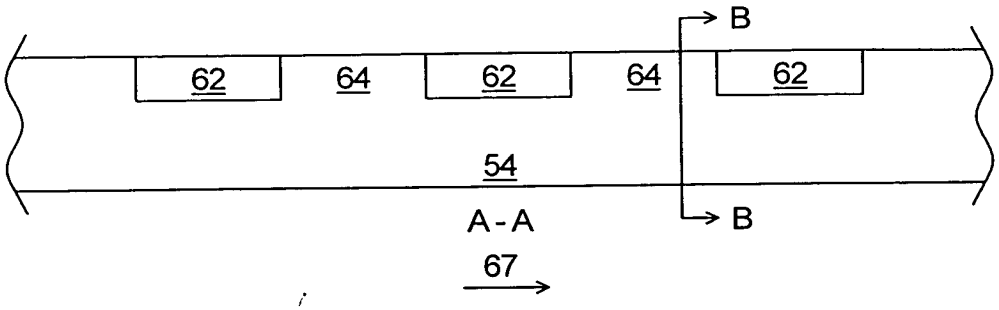


Figure 19a

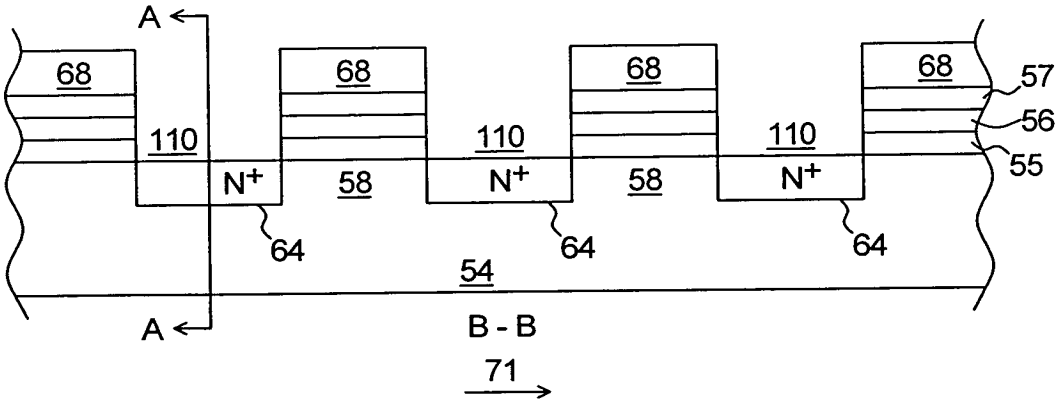


Figure 19b

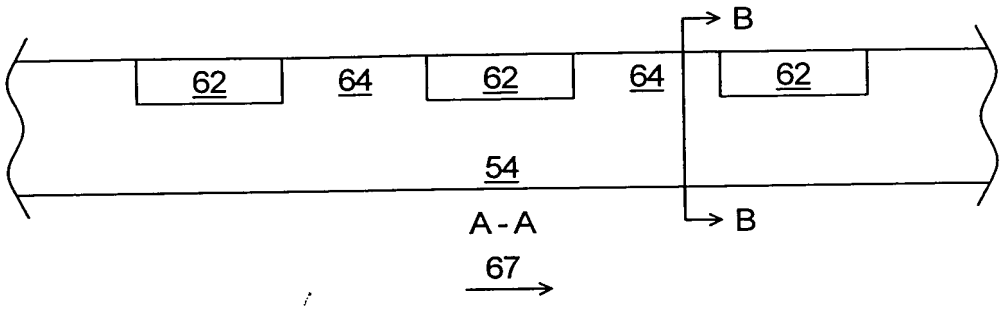


Figure 20a

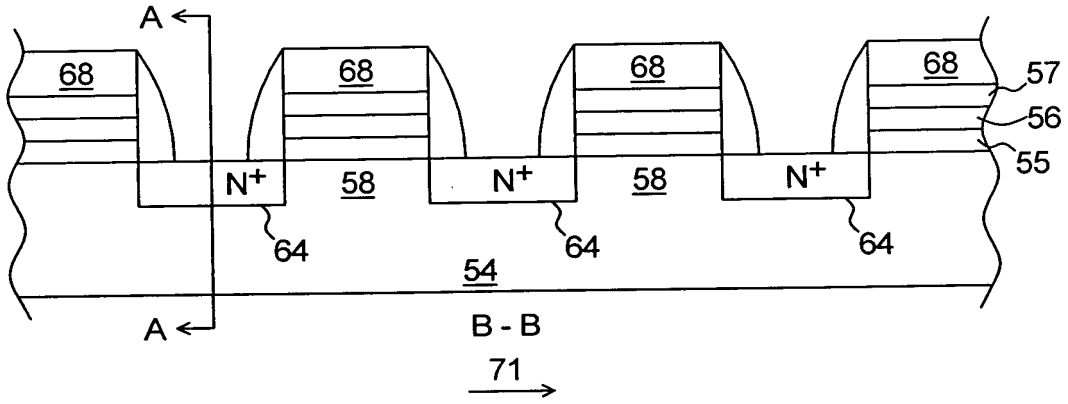
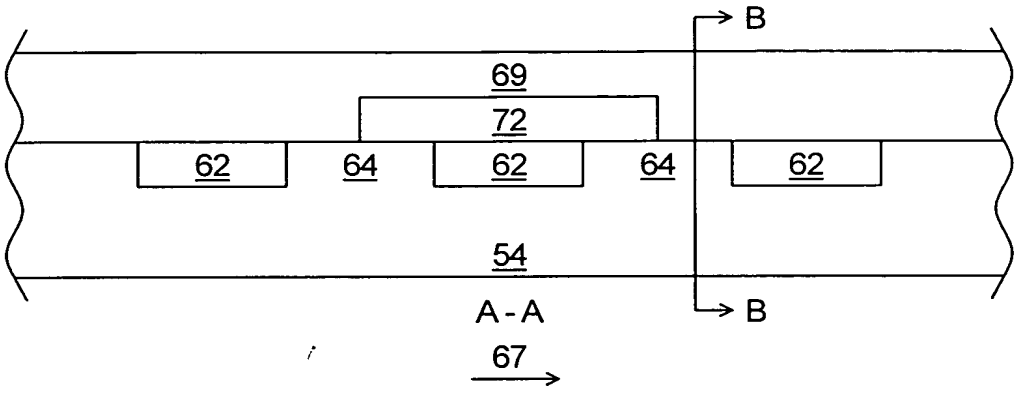


Figure 20b



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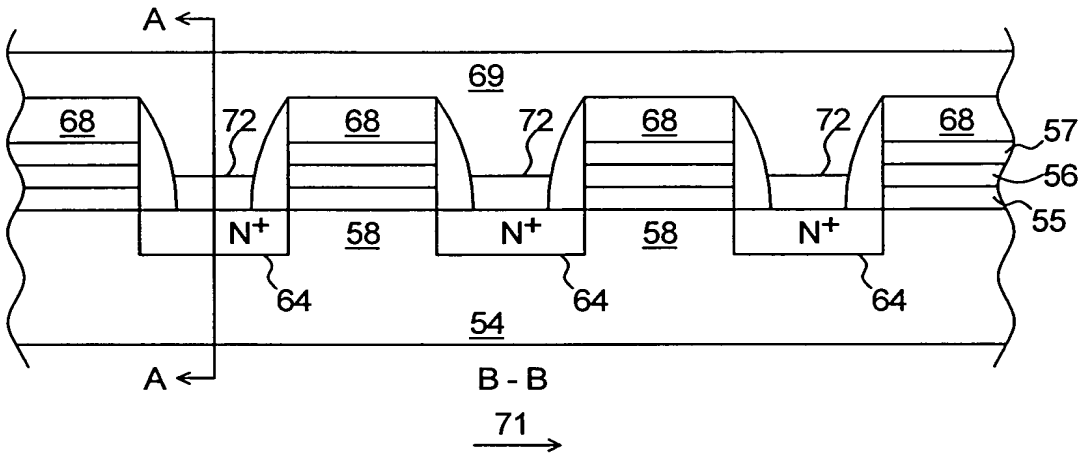


Figure 21b

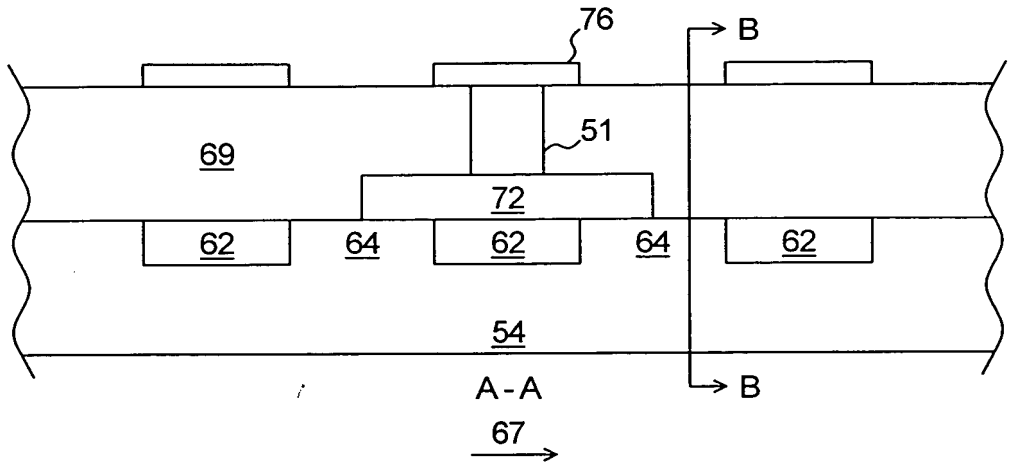


Figure 22a

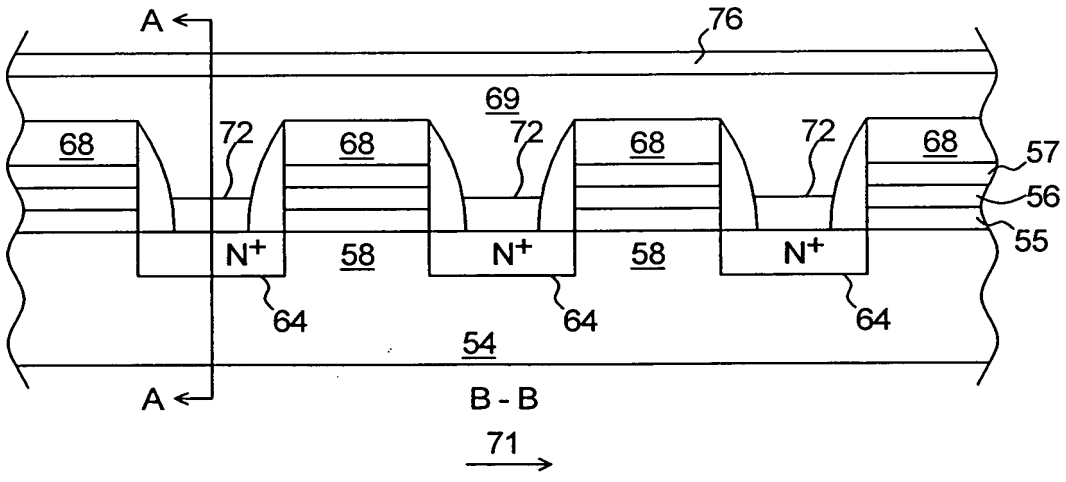
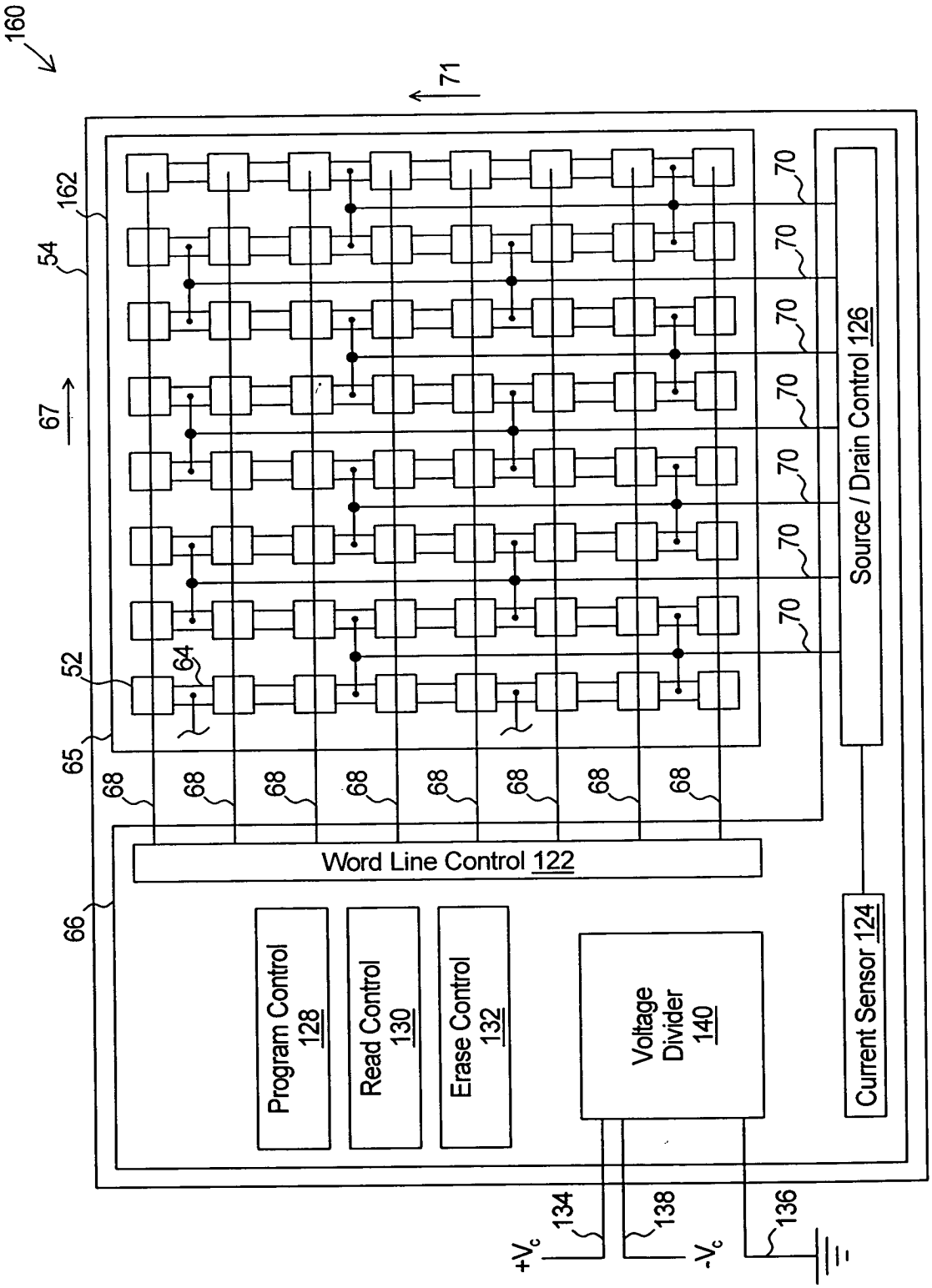


Figure 22b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Source / Drain Control 126
Word Line Control 122
Program Control 128
Read Control 130
Erase Control 132
Voltage Divider 140
Current Sensor 124
134
138
136
+Vc
-Vc

Figure 23